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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,450	02/26/2004	Garo J. Derderian	97-1252.01	7825

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EXAMINER	
MALDONADO, JULIO J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,450	DERDERIAN ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27* is/are allowed.

6)☒ Claim(s) *1-26 and 28-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20040226*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicants' cancellation of claims 28 and 49-72 is acknowledged.

2. Claims 1-48 are pending in the Application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 5, 6, 12, 13, 39-42 and 45-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsunemine (U.S. 5,699,291).

In reference to claims 1-3, 5, 6, 12, 13, 39-42 and 45-47, Tsunemine (Figs.1-18) teaches a method of forming a DRAM including an interconnect structure including the steps of providing a substrate (1); forming gate structures (3-5) on said substrates (1); forming contacts (7) on the substrate (1); forming an interlayer dielectric layer (11) on said substrate (1) including said gate structures (3-5) and said contacts (7); forming a contact hole (11a) in said interlayer dielectric layer (11) exposing said contacts (7); forming a polysilicon plug (12) in said contact hole (11a); recessing said polysilicon plug (12) to a distance (h) within said contact hole (11a); forming a barrier metal layer (13) made of Ti, W or Ta on said recessed polysilicon plug (11a) by a chemical vapor deposition process; forming a metal silicide layer (13e) by silicidizing said bottom of said

barrier metal layer (13); removing unreacted barrier metal layer (13); nitridizing said metal silicide layer (13e); forming a lower electrode (14); forming a capacitor dielectric layer (15); and forming a capacitor upper electrode (16), wherein said barrier layer has a higher concentration of silicon atoms at the bottom portion of said barrier than at the top of said barrier layer providing the further advantage of reduced contact resistance on the polysilicon plug (11a), and wherein said barrier layer has a higher concentration of nitrogen atoms at the top portion of said barrier than at the bottom portion (column 9, line 43 – column 11, line 65).

In reference to claim 48, Tsunemine substantially teaches all aspects of the invention, but fails to expressly teach reacting said barrier component with a portion of said silicon contact containing at least one oxygen atom. However, it is well known in the art that native oxides are formed after recessing a polysilicon plug as explained in Xing et al. to U.S. 6,090,697 (column 7, lines 62 – 67) Hwang et al. to U.S. 6,180,970 B1 (column 5, lines 41 – 56) and Sakoh to U.S. 5,641,991 (column 1, line 59 – column 2,line 32). Therefore, it is inherent that there is at least one oxygen atom in the polysilicon plug.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunemine (U.S. 5,699,291) in view of Xing et al. (U.S. 6,090,697).

Tsunemine (Figs.1-18) teaches a method of forming a DRAM including an interconnect structure including the steps of providing a substrate (1); forming gate structures (3-5) on said substrates (1); forming contacts (7) on the substrate (1); forming an interlayer dielectric layer (11) on said substrate (1) including said gate structures (3-5) and said contacts (7); forming a contact hole (11a) in said interlayer dielectric layer (11) exposing said contacts (7); forming a polysilicon plug (12) in said contact hole (11a); recessing said polysilicon plug (12) to a distance (h) within said contact hole (11a); forming a barrier metal layer (13) made of Ti, W or Ta on said recessed polysilicon plug (11a) by a chemical vapor deposition process; forming a metal silicide layer (13e) by silicidizing said bottom of said barrier metal layer (13); removing unreacted barrier metal layer (13); nitridizing said metal silicide layer (13e); forming a lower electrode (14); forming a capacitor dielectric layer (15); and forming a capacitor upper electrode (16), wherein said barrier layer has a higher concentration of silicon atoms at the bottom portion of said barrier than at the top of said barrier layer providing the further advantage of reduced contact resistance on the polysilicon plug (11a), and wherein said barrier layer has a higher concentration of nitrogen atoms at the top portion of said barrier than at the bottom portion (column 9, line 43 – column 11, line 65).

Tsunemine fails to teach wherein said polysilicon plug is a doped polysilicon plug. However, Xing et al. (Fig.2) teach a method of forming a DRAM including forming

a conductive plug (206) in a contact hole formed in an interlevel dielectric layer (202), wherein the conductive plug (206) is selected from a group that includes doped polysilicon (column 4, lines 2 – 44). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Tsunemine and Xing et al. to enable forming the polysilicon plug of Tsunemine according to the teachings of Xing because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed polysilicon plug of Tsunemine and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

7. Claims 7-9, 11, 14, 15, 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunemine (U.S. 5,699,291) in view of Nishioka et al. (U.S. 5,489,548).

Tsunemine (Figs.1-18) teaches a method of forming a DRAM including an interconnect structure including the steps of providing a substrate (1); forming gate structures (3-5) on said substrates (1); forming contacts (7) on the substrate (1); forming an interlayer dielectric layer (11) on said substrate (1) including said gate structures (3-5) and said contacts (7); forming a contact hole (11a) in said interlayer dielectric layer (11) exposing said contacts (7); forming a polysilicon plug (12) in said contact hole (11a); recessing said polysilicon plug (12) to a distance (h) within said contact hole (11a); forming a barrier metal layer (13) made of Ti, W or Ta on said recessed polysilicon plug (11a) by a chemical vapor deposition process; forming a metal silicide layer (13e) by silicidizing said bottom of said barrier metal layer (13); removing

unreacted barrier metal layer (13); nitridizing said metal silicide layer (13e); forming a lower electrode (14); forming a capacitor dielectric layer (15); and forming a capacitor upper electrode (16), wherein said barrier layer has a higher concentration of silicon atoms at the bottom portion of said barrier than at the top of said barrier layer providing the further advantage of reduced contact resistance on the polysilicon plug (11a), and wherein said barrier layer has a higher concentration of nitrogen atoms at the top portion of said barrier than at the bottom portion (column 9, line 43 – column 11, line 65).

Tsunemine fails to further include ruthenium oxide in the interconnect structure. However, Nishioka et al. (Figs.13 and 14) teach a method of forming a DRAM including the steps of forming a dielectric layer (32) over a substrate (30); forming a contact hole in said dielectric layer (32); forming a polysilicon plug (54) recessed in said contact hole; forming a titanium layer over said polysilicon plug; and nitridizing and silicidizing said titanium layer to form a TiN/$TiSi_2$/poly silicon structure (54, 34, 36). Nishioka also teaches alternate materials for the TiN/$TiSi_2$/poly silicon structure, such as ruthenium oxide, TaN, TiSiN, etc., and combinations of the materials (Nishioka, column 7, line 12 – column 8, line 38). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Tsunemine and Nishioka et al. to enable forming the interconnect structure of Tsunemine according to the teachings of Nishioka et al. because one of ordinary skill in the art would have been motivated to look to alternative suitable methods of forming the disclosed interconnect of Tsunemine and art

recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunemine (U.S. 5,699,291) in view of Nishioka et al. (U.S. 5,489,548) as applied to claims 7-9, 11, 14, 15, 20-24 above, and further in view of Yeh (U.S. 5,410,185).

The combined teachings of Tsunemine and Nishioka et al. substantially teach all aspects of the invention but fail to disclose wherein said chemical vapor deposition process is selective chemical vapor deposition. However, Yeh (Figs.5-9) teach depositing a metal layer (16) such as tungsten or any other refractory metal by either blanket or selective chemical vapor deposition (column 5, lines 7 – 21). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Tsunemine and Nishioka et al. with Yeh to enable the depositing step of Tsunemine and Nishioka et al. to be performed according to the teachings of Yeh because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed depositing step of Tsunemine and Nishioka et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

9. Claims 16-19, 36-38, 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunemine (U.S. 5,699,291) in view of Yeh (U.S. 5,410,185).

Tsunemine (Figs.1-18) teaches a method of forming a DRAM including an interconnect structure including the steps of providing a substrate (1); forming gate structures (3-5) on said substrates (1); forming contacts (7) on the substrate (1); forming

an interlayer dielectric layer (11) on said substrate (1) including said gate structures (3-5) and said contacts (7); forming a contact hole (11a) in said interlayer dielectric layer (11) exposing said contacts (7); forming a polysilicon plug (12) in said contact hole (11a); recessing said polysilicon plug (12) to a distance (h) within said contact hole (11a); forming a barrier metal layer (13) made of Ti, W or Ta on said recessed polysilicon plug (11a) by a chemical vapor deposition process; forming a metal silicide layer (13e) by silicidizing said bottom of said barrier metal layer (13); removing unreacted barrier metal layer (13); nitridizing said metal silicide layer (13e); forming a lower electrode (14); forming a capacitor dielectric layer (15); and forming a capacitor upper electrode (16), wherein said barrier layer has a higher concentration of silicon atoms at the bottom portion of said barrier than at the top of said barrier layer providing the further advantage of reduced contact resistance on the polysilicon plug (11a), and wherein said barrier layer has a higher concentration of nitrogen atoms at the top portion of said barrier than at the bottom portion (column 9, line 43 – column 11, line 65).

Tsunemine fails to teach reducing said poly plug to half of said length. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere

dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Still, Tsunemine fail to disclose wherein said chemical vapor deposition process is selective chemical vapor deposition. However, Yeh (Figs.5-9) teach depositing a metal layer (16) such as tungsten or any other refractory metal by either blanket or selective chemical vapor deposition (column 5, lines 7 – 21). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Tsunemine and Yeh to enable the depositing step of Tsunemine to be performed according to the teachings of Yeh because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed depositing step of Tsunemine and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

10. Claims 25, 26 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunemine (U.S. 5,699,291) in view of Xing et al. (U.S. 6,090,697) and Yeh (U.S. 5,410,185).

Tsunemine (Figs.1-18) teaches a method of forming a DRAM including an interconnect structure including the steps of providing a substrate (1); forming gate structures (3-5) on said substrates (1); forming contacts (7) on the substrate (1); forming

an interlayer dielectric layer (11) on said substrate (1) including said gate structures (3-5) and said contacts (7); forming a contact hole (11a) in said interlayer dielectric layer (11) exposing said contacts (7); forming a polysilicon plug (12) in said contact hole (11a); recessing said polysilicon plug (12) to a distance (h) within said contact hole (11a); forming a barrier metal layer (13) made of Ti, W or Ta on said recessed polysilicon plug (11a) by a chemical vapor deposition process; forming a metal silicide layer (13e) by silicidizing said bottom of said barrier metal layer (13); removing unreacted barrier metal layer (13); nitridizing said metal silicide layer (13e); forming a lower electrode (14); forming a capacitor dielectric layer (15); and forming a capacitor upper electrode (16), wherein said barrier layer has a higher concentration of silicon atoms at the bottom portion of said barrier than at the top of said barrier layer providing the further advantage of reduced contact resistance on the polysilicon plug (11a), and wherein said barrier layer has a higher concentration of nitrogen atoms at the top portion of said barrier than at the bottom portion (column 9, line 43 – column 11, line 65).

Tsunemine fails to teach wherein said polysilicon plug is a doped polysilicon plug. However, Xing et al. (Fig.2) teach a method of forming a DRAM including forming a conductive plug (206) in a contact hole formed in an interlevel dielectric layer (202), wherein the conductive plug (206) is selected from a group that includes doped polysilicon (column 4, lines 2 – 44). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Tsunemine and Xing et al. to enable forming the polysilicon plug of Tsunemine according to the teachings of Xing because

one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed polysilicon plug of Tsunemine and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Still, the combined teachings of Tsunemine and Xing et al. fail to disclose wherein said chemical vapor deposition process is selective chemical vapor deposition. However, Yeh (Figs.5-9) teach depositing a metal layer (16) such as tungsten or any other refractory metal by either blanket or selective chemical vapor deposition (column 5, lines 7 – 21). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Tsunemine and Xing et al. with Yeh to enable the depositing step of Tsunemine and Xing et al. to be performed according to the teachings of Yeh because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed depositing step of Tsunemine and Xing et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

11. Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunemine (U.S. 5,699,291) in view of Xing et al. (U.S. 6,090,697) and Yeh (U.S. 5,410,185) as applied to claims 25, 26 and 29-31 above, and further in view of Nishioka et al. (U.S. 5,489,548).

The combined teachings of Tsunemine, Xing et al. and Yeh substantially teach all aspects of the invention but fail to teach forming an oxygen barrier over said silicon barrier. However, Nishioka et al. (Figs.13 and 14) teach a method of forming a DRAM

including the steps of forming a dielectric layer (32) over a substrate (30); forming a contact hole in said dielectric layer (32); forming a polysilicon plug (54) recessed in said contact hole; forming a titanium layer over said polysilicon plug; and nitridizing and silicidizing said titanium layer to form a TiN/$TiSi_2$/poly silicon structure (54, 34, 36). Nishioka also teaches alternate materials for the TiN/$TiSi_2$/poly silicon structure, such as ruthenium oxide (an oxygen barrier material), TaN, TiSiN, etc., and combinations of the materials (Nishioka, column 7, line 12 – column 8, line 38). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Tsunemine, Xing et al. and Yeh with Nishioka et al. to enable forming the interconnect structure of Tsunemine, Xing et al. and Yeh according to the teachings of Nishioka et al. because one of ordinary skill in the art would have been motivated to look to alternative suitable methods of forming the disclosed interconnect of Tsunemine, Xing et al. and Yeh and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

12. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunemine (U.S. 5,699,291) in view of Xing et al. (U.S. 6,090,697).

Tsunemine (Figs.1-18) teaches a method of forming a DRAM including an interconnect structure including the steps of providing a substrate (1); forming gate structures (3-5) on said substrates (1); forming contacts (7) on the substrate (1); forming an interlayer dielectric layer (11) on said substrate (1) including said gate structures (3-5) and said contacts (7); forming a contact hole (11a) in said interlayer dielectric layer (11) exposing said contacts (7); forming a polysilicon plug (12) in said contact hole

(11a); recessing said polysilicon plug (12) to a distance (h) within said contact hole (11a); forming a barrier metal layer (13) made of Ti, W or Ta on said recessed polysilicon plug (11a) by a chemical vapor deposition process; forming a metal silicide layer (13e) by silicidizing said bottom of said barrier metal layer (13); removing unreacted barrier metal layer (13); nitridizing said metal silicide layer (13e); forming a lower electrode (14); forming a capacitor dielectric layer (15); and forming a capacitor upper electrode (16), wherein said barrier layer has a higher concentration of silicon atoms at the bottom portion of said barrier than at the top of said barrier layer providing the further advantage of reduced contact resistance on the polysilicon plug (11a), and wherein said barrier layer has a higher concentration of nitrogen atoms at the top portion of said barrier than at the bottom portion (column 9, line 43 – column 11, line 65).

Tsunemine fails to teach wherein said polysilicon plug is a doped polysilicon plug. However, Xing (Figs.2 and 3) teach a method of forming a DRAM including providing a substrate (300); forming a first dielectric layer (302) on said substrate (300); forming a contact hole in said first dielectric layer (302); forming a doped polysilicon plug (306) in said contact hole; forming a second insulation layer over said first insulation layer; and forming a second hole in said second insulation layer. However, Xing et al. (Fig.2) teach a method of forming a DRAM including forming a conductive plug (206) in a contact hole formed in an interlevel dielectric layer (202), wherein the conductive plug (206) is selected from a group that includes doped polysilicon (column 4, lines 2 – 44). Furthermore, Xing et al. (Figs.2 and 3) teach wherein said capacitor

used to form said DRAM is formed by patterning a first electrode layer (204), forming a capacitor dielectric (212), and forming a second electrode (214); or by forming a second insulation layer (316), forming a hole in said second insulation layer (316); and forming a first electrode layer (304), the capacitor dielectric layer (312) and second electrode layer (314), wherein said second hole includes an adhesion promoting layer (210, 310) which can be used as an oxidation barrier (column 4, line 1 – column 6, line 26 and column 7, line 62 – column 8, line 18).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Tsunemine and Xing et al. to enable forming the polysilicon plug of Tsunemine according to the teachings of Xing because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed polysilicon plug of Tsunemine and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07. I would also be obvious to one of ordinary skill in the art at the time the invention was made to enable making the capacitor of the DRAM disclosed in Tsunemine to arrive at the claimed invention.

Allowable Subject Matter

13. Claim 27 is allowed.

Conclusion

14. Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (http://portal.uspto.gov/external/portal/pair) which provides

applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

16. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this group is 571-273-8300. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
August 2, 2005

George Fourson
Primary Examiner